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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/715,081	11/20/2000	Akitaka Nakayama	001542	7823
7.	590 09/10/2002			
ARMSTRONG, WESTERMAN, HATTORI, McLELAND & NAUGHTON Suite 1000 1725 K Street, N.W. Washington, DC 20006			EXAMINER	
			SHAPIRO, JEFFERY A	
			ARTONII	PAPER NUMBER
•			DATE MAILED: 09/10/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary The MAILING DATE of this communication appearage of the second for Reply A SHORTENED STATUTORY PERIOD FOR REPLY	IS SET TO EXPIRE 3 MONTH(sec.) (a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days apply and will expire SIX (6) MONTHS from the statutory of the statutory minimum of the statu	S) FROM sely filed s will be considered timely.				
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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1)⊠ Responsive to communication(s) filed on 20 No	ovember 2000 .					
2a) ☐ This action is FINAL . 2b) ☒ This	action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disp sition of Claims						
4)⊠ Claim(s) <u>1-10</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-10</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) accepte	•	'				
Applicant may not request that any objection to the c		• •				
11) The proposed drawing correction filed on is		ved by the Examiner.				
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
 Certified copies of the priority documents have been received. Certified copies of the priority documents have been received in Application No. 						
Copies of the certified copies of the priority documents have been received in Application No Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) The translation of the foreign language provisional application has been received. 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing R view (PTO-948) 3) Information Disclosure Stat ment(s) (PTO-1449) Pap r No(s)	5) Notice of Informal P	(PTO-413) Paper No(s) latent Application (PTO-152)				

Application/Control Number: 09/715,081 Page 2

Art.Unit: 3653

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- 2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant in lines 7 and 8 by the phrase "printed wiring boards of fraction which should be laid out." See also lines 16-18 as well. It is also unclear in line 10 what is meant by "different kind from multiple kinds." In addition, it is not clear what is "according to multiple manufacturing schedule data." For example, is the detecting unit detecting according to schedule data or are the wiring boards scheduled to be manufactured according to schedule data?
- 3. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 3653

5. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura. Kitamura discloses the manufacturing system for printed wiring boards as follows.

As described in Claims 1, 9 and 10;

- 1. a schedule data storage unit (302) storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;
- 2. a detecting unit (205) detecting a quantity of printed wiring boards which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing schedule data (note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment);
- a condition data storage unit (204) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block;
- 4. a dividing unit dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data (note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of

Art Unit: 3653

processing equipment based on the product information, the equipment information and process information);

5. a determining unit determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group (note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information);

As described in Claim 2;

6. said detecting unit, if a manufacturing quantity of the boards of a certain kind cannot be divided completely by a maximum number of the boards which can be laid out in a single predetermined manufacturing block, detects printed wiring boards corresponding to a number smaller than said maximum number or an excess of boards of said fraction (again, note that such a system as that of Kitamura necessarily maximizes the most product that can fit on a particular machine so as to efficiently process the required product as determined by customer orders);

As described in Claim 3;

7. the manufacturing condition data is data produced by combining orders with product data (note that customer orders and product data are necessarily combined in order to move material through the system—see also manufacturing situation memory (1105) and product information

Art Unit: 3653

memory (1103), which are both used to optimize work flow through the production line);

As described in Claim 4;

8. the order data includes a shipment date (note that it is inherent and obvious that product moving through the system would have a shipment date assigned to it);

As described in Claims 5 and 6;

- 9. the product data includes the number of layers of the printed wiring boards (note that it would be obvious to include the number of layers as design and processing parameters since the process of Kitamura is for semiconductor manufacturing—see abstract, lines 1 and 2);
- 6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Shin et al. Kitamura discloses the system as described above.

 Kitamura does not expressly disclose, but Shin et al discloses the following.

As described in Claim 7;

- a CAD data creating unit (see col. 17, lines 21-23) creating CAD
 data corresponding to a combination determined by said determining unit;
- 11. a CAD data converting unit creating CAM data or CAT data corresponding to CAD data created by said CAD data creating unit (see col. 17, lines 21-47);

Art Unit: 3653

As described in Claim 8;

12. a manufacturing unit group (20, 22, 24, 26 and 28) carrying out a manufacturing process for the printed wiring board using the CAM data or the CAT data created by said CAD data creating unit;

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the CAD and CAT creating units and converting units to create product and test data, as described by Shin et al, for use by the system of Kitamura.

The suggestion/motivation would have been to provide direct input of product information required for production and testing of PC-Boards.

Therefore, it would have been obvious to combine Kitamura and Shin et al in order to obtain the invention as specified in Claims 7 and 8.

Conclusion

- 7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jain et al, Glaser et al, Tanaka et al, Hino et al, Arai et al, Chaiken et al, and Fujino et al are all cited as examples of PCB manufacturing systems or general production systems. In addition, Chaiken et al discloses maximization of material layout on a flat, planar piece of material.
- 8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (703)308-3423. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 3600

Application/Control Number: 09/715,081

Art Unit: 3653

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald P. Walsh can be reached on (703)306-4173. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-2571 for regular communications and (703)308-2571 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-1113.

Jeffrey A. Shapiro Patent Examiner,

Art Unit 3653

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September 4, 2002